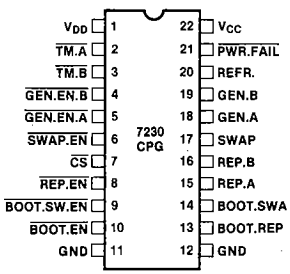
7230
CURRENT PULSE GENERATOR FOR BUBBLE MEMORIES

- **TTL Compatible Inputs**
- **Provides all Pulses for IM's Bubble Memories**
  - **— Replicate, Swap, Generate, Boot Replicate and Bootswap**
- **Current Sink Outputs Designed to Directly Drive Bubble Memory**
- **Direct Interface to Bubble Memory Controller**
- **Automatic Power Fail and Reset**
- **Operates from +5 and +12 Volts Only**
- **Schottky Bipolar Technology**
- **Standard 22-Pin Dual-In-Line Package**

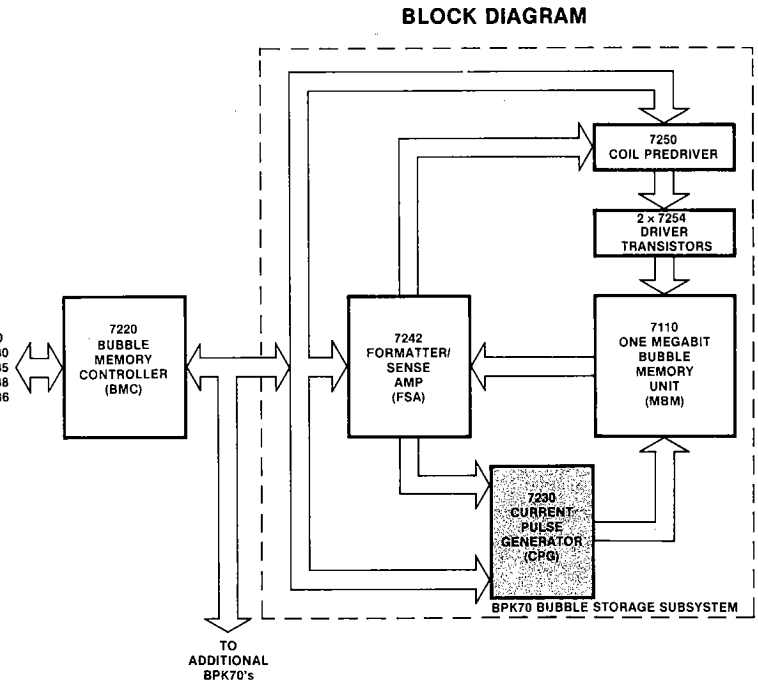
The Intel 7230 is a Current Pulse Generator (CPG) designed to drive Intel Magnetics Bubble Memories. The 7230 is a Schottky Bipolar, TTL input compatible device that converts digital timing signals to analog current pulses. The CPG provides all pulses for Intel Magnetics Bubble Memories (7110 Family). These include Replicate, Swap, Generate, Boot Replicate and Bootswap pulses. The high current sinking outputs directly drive the bubble memory. It also directly interfaces to the Intel Magnetics Bubble Memory Controller (7220) and Formatter/Sense amplifier (7242).

The 7230 operates from 5-volt and 12-volt power supplies and is in a standard 22-pin dual-in-line package.

PIN CONFIGURATION

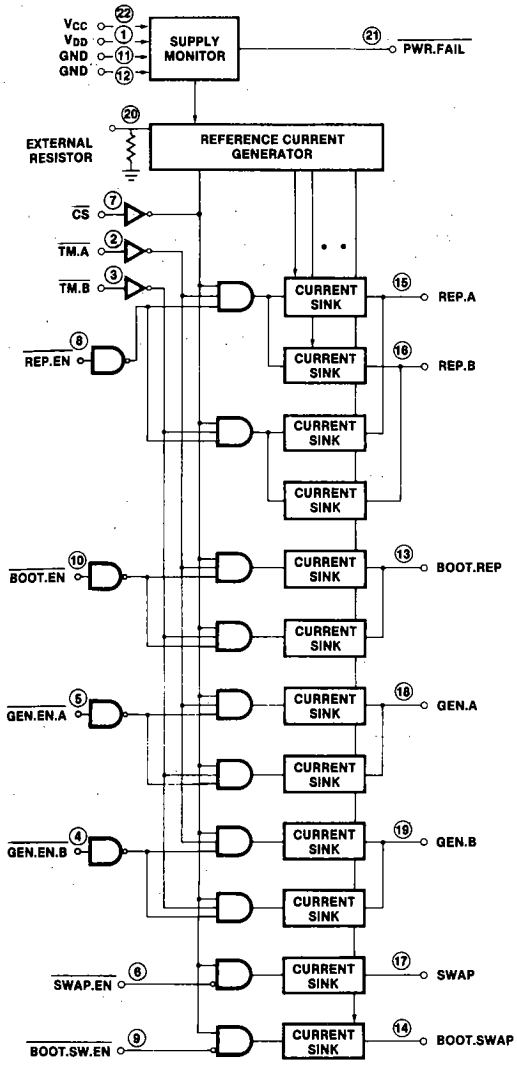


BLOCK DIAGRAM



Block Diagram of Single Bubble Memory System — 128K Bytes

LOGIC DIAGRAM



EXTERNAL RESISTOR REQUIREMENTS

Connect a 1% resistor based on the following table between pin 20 and ground.

7230 Marking	External Resistor
S6590	3.48K

PIN DESCRIPTION

$\overline{\text{BOOT.EN}}$ (Pin 10)
An active low input enabling the BOOT.REP output current pulse.

BOOT.REP (Pin 13)
An output providing the current pulse for bootstrap loop replication in the bubble memory.

BOOT.SWAP (Pin 14)
An output providing a current pulse which may be used for writing data into the bootstrap loop.

$\overline{\text{BOOT.SW.EN}}$ (Pin 9)
An active low input enabling the BOOT.SWAP output current pulse.

$\overline{\text{CS}}$ (Pin 7)
An active low input for selecting the chip. The chip powers down during deselect.

GEN.A (Pin 18)
An output providing the current pulse for writing data into the "A" quads of the bubble memory.

GEN.B (Pin 19)
An output providing the current pulse for writing data into the "B" quads of the bubble memory.

$\overline{\text{GEN.EN.A}}$ (Pin 5)
An active low input enabling the GEN.A output current pulse.

$\overline{\text{GEN.EN.B}}$ (Pin 4)
An active low input enabling the GEN.B output current pulse.

$\overline{\text{PWR.FAIL}}$ (Pin 21)
An active low, open collector output indicating that either V_{CC} or V_{DD} is below its threshold value.

REFR. (Pin 20)
The pin for the reference current generator to which an external resistance must be connected.

REP.A (Pin 15)
An output providing the current pulse for replication of data in the "A" quads of the bubble memory.

REP.B (Pin 16)
An output providing the current pulse for replication of data in the "B" quads of the bubble memory.

$\overline{\text{REP.EN}}$ (Pin 8)
An active low input enabling the REP.A and REP.B outputs.

PIN DESCRIPTION (continued)

SWAP (Pin 17)

An output providing the current pulse for exchanging the data between the input track and the storage loops in the bubble memory.

$\overline{\text{SWAP.EN}}$ (Pin 6)

An active low input enabling the SWAP output.

$\overline{\text{TM.A}}$ (Pin 2)

An active low timing signal determining the cut pulse widths of the BOOT.REP, GEN.A, GEN.B, REP.A and REP.B outputs.

$\overline{\text{TM.B}}$ (Pin 3)

An active low timing signal determining the transfer pulse widths of the BOOT.REP, GEN.A, GEN.B, REP.A and REP.B outputs.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −20°C to +80°C
Storage Temperature ..... −65°C to +150°C
V_{CC} and Input Voltages ..... −0.5V to +7V
V_{DD} and Output Voltages ..... −0.5V to +14V
Power Dissipation 1W
$\overline{\text{Power Fail}}$ Output Sink Current 10mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$, $V_{DD} = 12V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_{IL}	Input Low Current			−0.4	mA	$V_{IL} = 0.4V$, $V_{CC} = 5.25V$
I_{IH}	Input High Current			20	μA	$V_{IH} = V_{CC} = 5.25V$
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_C	Input Clamp Voltage			−1.5	V	$I = -18$ mA, $V_{CC} = 4.75V$
I_{CEX1}	Output Leakage Current (All Outputs except $\overline{\text{PWR.FAIL}}$)			1.0	mA	$V_{CC}=5.25V$, $V_{DD}=12.6V$
I_{CEX2}	$\overline{\text{PWR.FAIL}}$ Output Leakage Current			100	μA	$V_{OH} = V_{CC} = 5.25V$
V_{OL}	$\overline{\text{PWR.FAIL}}$ Output Low Voltage			0.4	V	$I_{OL} = 4$ mA, $V_{CC} = 4.75V$
V_{CCTH}	V_{CC} Threshold (for $\overline{\text{PWR.FAIL}}$)		4.65		V	$V_{DD} = 12V$
V_{DDTH}	V_{DD} Threshold (for $\overline{\text{PWR.FAIL}}$)		11.3		V	$V_{CC} = 5V$
I_{CC1}	Current from V_{CC} — Selected		30	45	mA	$CS = V_{IL}$, $V_{CC} = 5.25V$
I_{DD1}	Current from V_{DD} — Selected		20	35	mA	$CS = V_{IL}$, $V_{DD} = 5.25V$
I_{DD2}	Current from V_{DD} — Power Down		6	16	mA	$CS = V_{IH}$, $V_{DD} = 12.6V$

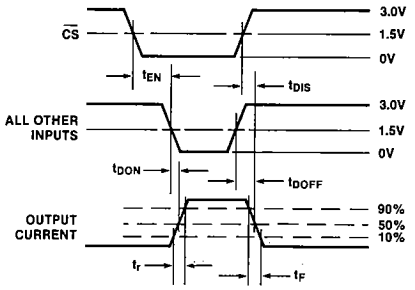
A.C. CHARACTERISTICS

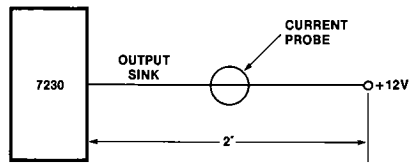
$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$, $V_{DD} = 12V \pm 5\%$.

Symbol	Parameter	Min.	Max.	Unit	Test Conditions*
t_{DON}	Propagation Delay (Turn On)	50	100	ns	
t_{DOFF}	Propagation Delay (Turn Off)	20	50	ns	
t_r	Output Current Rise Time		160	ns	See Test Setup Below
t_f	Output Current Fall Time		20	ns	See Test Setup Below
t_{DIS}	$\overline{\text{CS}}$ Disable Time		50	ns	
t_{EN}	$\overline{\text{CS}}$ Enable Time		500	ns	

*Note: $V_{CC} = 4.5V$ and $V_{DD} = 10.8V$ for all tests.

WAVEFORMS





Test Setup for Output Current Rise and Fall Time Measurement

CAPACITANCE*

$T_A = 25°C$.

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions*
C_{IN}	Input Capacitance		10	pF	

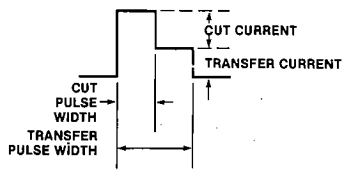
*This parameter is periodically sampled and not 100% tested. Condition of measurement is f = 1 MHz.

OUTPUT CURRENTS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5.0V \pm 5\%$, $V_{DD} = 12.0V \pm 5\%$

Output ($V_{OUT} = 3.0V$)	Nominal Values at 50 KHz	
	Current (mA)	Pulse Width (μs)
	S6590	S6590
REP.A, REP.B CUT	180	0.25
REP.A, REP.B TRANSFER	140	5.0
BOOT.REP CUT	90	0.25
BOOT.REP TRANSFER	70	5.0
GEN.A, GEN.B CUT	64	0.25
GEN.A, GEN.B TRANSFER	36	5.0
SWAP	120	28.75
BOOT.SWAP	70	See Note

Two-level pulses are defined as shown:



Note: Writing data into the bootstrap loop would require 4096 pulses of 20μs width.